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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,755	06/05/2006	Jiangqi He	10/581,755	8391

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
01/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,755	HE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 18-32* is/are pending in the application.

4a) Of the above claim(s) *18-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 25-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/7/06,7/10/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Applicant's election of claims 1-9,25-32 for prosecution without traverse in the communication with the Office on November 27th 2009 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claim 1,4,7,9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al. (U.S. Patent 6,281,042) thereafter Ahn 042

With regard to claim 1, Ahn 042 discloses (fig 3) a microelectronic device comprising: a package substrate having a first side and an opposing second side; a microprocessor adjacent to

the first side of the package substrate(column 1 lines 64-67; column 2 lines 1-10) and

a memory device adjacent to the second side of the package substrate (column 2 lines 1-10 ,

wherein the package substrate is electrically coupled to at least one of the microprocessor and the memory device.

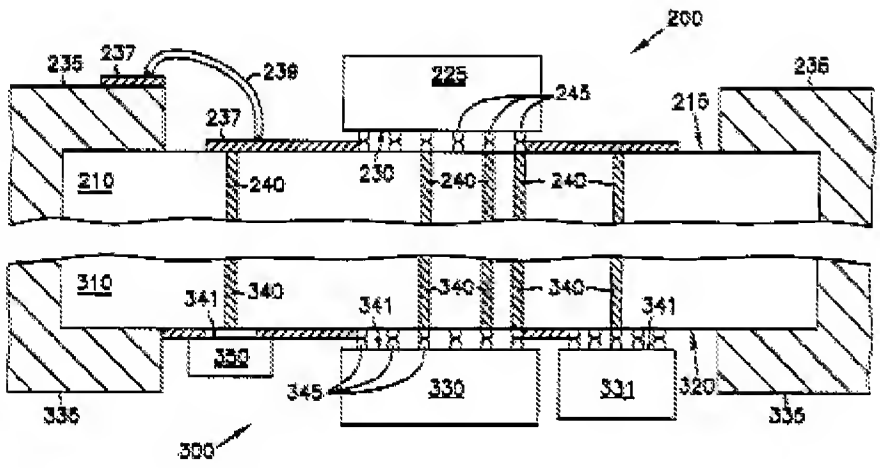

FIG 4 OF AHN 042 DISCLOSURES

With regard to claim 4 , Ahn 042 discloses (fig 4) a microelectronic device wherein the second die disposed on a land side of the substrate (note that Ahn 042 discloses a land side on both surface of the substrate

With regard to claim 7, Ahn 042 discloses (fig 4) a microelectronic device further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.

With regard to claim 9, Ahn 042 discloses a microelectronic device further including an integrated heat spreader thermally coupled to one or more of the die.(column 5 lines 30-36)

4. Claim 1,4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilmour et al. (U.S. Patent 5,391,917) thereafter Gilmour 917

With regard to claim 1, Gilmour 917 discloses (fig 7,) a microelectronic device comprising: a package substrate having a first side and an opposing second side; a microprocessor adjacent to the first side of the package substrate(fig 7 element 41) and a memory device adjacent to the second side of the package substrate (fig 7 element 73) , wherein the package substrate is electrically coupled to at least one of the microprocessor and the memory device.

With regard to claim 4 , Gilmour 917 discloses (fig 7) a microelectronic device wherein the second die disposed on a land side of the substrate (note that Gilmour 917 discloses a land side on both surface of the substrate)

With regard to claim 5, Gilmour 917 discloses (fig 8, fig 10,fig 11) a microelectronic device further comprising a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.

With regard to claim 6, Gilmour 917 discloses (fig 8, fig 10,fig 11) second die electrically coupled by one selected from the group including a wire bond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.

With regard to claim 7, Gilmour 917 discloses (fig 7,fig 9,fig 10,fig 11) a microelectronic device further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.

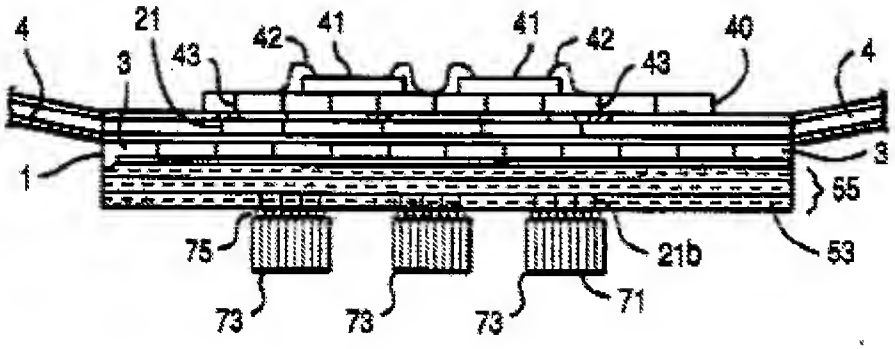

FIG. 7

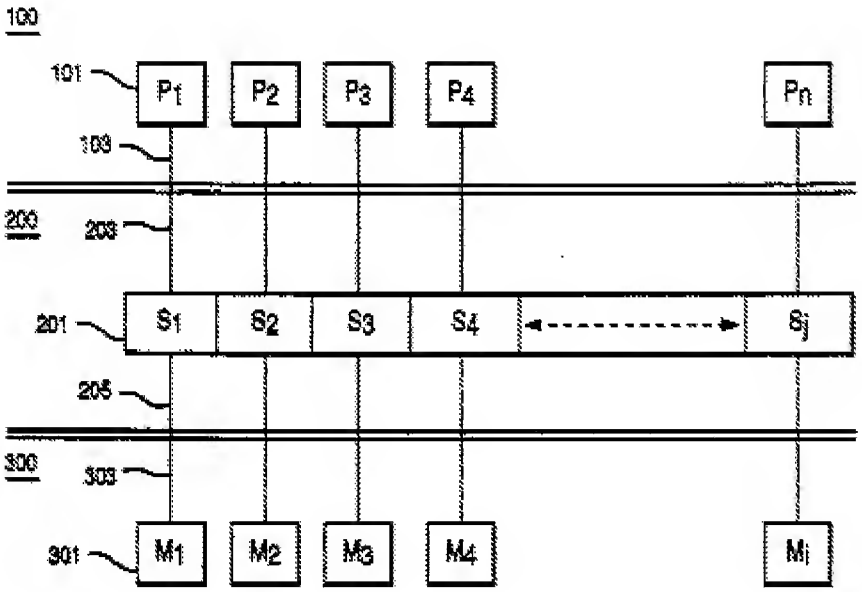

FIG. 11

Claim Rejections - 35 USC § 103

5. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2,3 ,27,28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (U.S. Patent 6,281,042) thereafter Ahn 042.

With regard to claim 2, as set forth in the rejection of claim 1, Ahn 042 discloses all the invention including a memory controller electrically coupled to the memory device (fig 4 column 6 lines 35-47) except for the specific that the memory controller is also integrated with the substrate that has the microprocessor and the memory device.

This limitation ,however, is considered obvious because the semiconductor chip 331 in Ahn 042 disclosure can be a memory controller. Furthermore , a person skilled in the art at the time the invention was made would have been motivated to incorporate a memory controller to increase the functionality of the Ahn 042 device and make it a commercial success.

With regard to claim 3 , as set forth in the rejection of claim 1, this claim is obvious because Ahn discloses a capacitor attached to the interposer and it has been held that the term " integral " is sufficiently broad enough to embraced construction united by such means as fastening and welding. In Re Honte 177 USPQ 326, 328 (CCPA1973). More over the used of embedded capacitor in a substrate (i.e. integral to the substrate is known in the art at the time the invention was made.) a disclosed by Iijima et al. (US patent 6,914,322) a person skilled in the art at the time the invention was made would have been motivated to incorporate an embedded capacitor in Ahn 042 device in order to increase the efficiency and functionality and make it a commercial success .

With regard to claim 27,28, as set forth in the rejection of claim 1, Ahn 042 discloses all the invention except for the specific use of Land Grid Array (LGA) or Pin Grid Array (PGA). Ahn 042 disclosed a structure of a Ball Grid Array (BGA) (column 5 lines 1-17) connection. and a BGA is an equivalent connection for LGA and PGA and therefore make claim 27,28 obvious over Ahn 042. Furthermore, a person skilled in the art at the time the invention was

made would have been motivated to provide more option for the Ahn 042 in order to increase its market share and make it a commercial success.

7. Claims 8, ,29, 25 ,26,30-32 are rejected under 35 U.S.C. 103 (a) as being unpatentable over by Gilmour et al. (U.S. Patent 5,391,917) thereafter Gilmour 917.

With regard to claim 8,29 as set forth in the rejection of claim 1, as set forth in the rejection of claim 7, Gilmour 917. discloses all the invention including a cache die (fig 10 ,chip 61, column 7 lines 1-9. except for the inclusion of a fourth level cache memory.

This limitation , however, is s considered obvious because the increasing the level of cache memory allow slower low cost small size memory element physically separate from the microprocessor to increase the speed and the throughput of the system is known in the art at the time the invention was made.(see the disclosure by Klein et al US patent Application Publication US 2004/0225821)

With regard to claims 25,26,30 , as set forth in the rejection of claim 8,25,29 Gilmour 917 discloses all the invention except for the limitation as recited in claims 25,26,30.

Those limitations ,however, are considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the

particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).***

With regard to claim 31, as set forth in the rejection of claim 29, Gilmour 917 disclosed all the invention. except for a third level cache with speed faster than system memory bus and the capacity of the fourth level cache .

These limitations, however, are considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).***

Furthermore , the use of Level three cache is known in the art at the time the invention was made . A person skilled in the art at the time would have been motivated to use a third level cache to allow the Gilmour 917 device to use different type of memory with different speed and size.

With regard to claim 32, as set forth in the rejection of claim 31, Gilmour 917 discloses all the invention except for the use of land grid array or pin grid array. This limitation ,however is considered obvious because the Examiner takes Official Notice that the use of a Land Grid Array (LGA) or a Pin Grid Array in a microprocessor package is known for a person skilled in the art at the time the invention was made.

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period

for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

10. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6:30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T. Nguyen/

Patent Examiner
Art Unit 2818